Enting Zhang

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Summary

Network Software Engineer specialized in **formal concurrency verification** and system-level observability. Creator of the **Clotho Verification Engine**, an independently developed orchestrator that explores concurrent state spaces via **Source-DPOR** and AST instrumentation. Proven expert in **Knowledge Recovery** within undocumented legacy environments, having decoded complex control plane internals into formal specifications for high-impact system transitions. Architect of **Project Oracle**, which slashed diagnostic TTR for core FIB issues from **4 hours to <3 seconds** by grounding AI-native reasoning in low-level system states.

Technical Skills

Formal Verification: Source-DPOR (Abdulla et al.), Vector Clocks (Lamport), Mazurkiewicz Traces, LTL Invariants.
Low-Level & Systems: Bare-metal C (C11), GDB Python API, AST Instrumentation, Memory Layout Optimization.
AI-Native Engineering: Tool-Use Orchestration, CausalRAG, Agentic Workflows, MCP, Genetic Programming.
Infrastructure: Python, Docker, Golang, AWS (DynamoDB), SQLite (SAVEPOINT-based state rollback).

Experience

Ciena Ottawa, ON
Network Software Engineer (Core Infrastructure & Verification) *May 2023 – Present*

- **Project Oracle (AI-Native Diagnostic Suite Interactive Demo):** Independently architected a 3-in-1 AI dev suite that establishes JSON as the "lingua franca" for in-memory C states. Integrated a **GDB-based Wireshark** for message tracing and a dynamic DB View that **slashed diagnostic TTR** for FIB sync issues from 4 hours to **<3 seconds**. Captured human heuristics for training data.
- **LTL-Driven Test Factory:** Architected a group theory generator permutation-based Unit Test framework for the core FIB module, auto-generating **8,084 high-fidelity tests (140K+ LoC)**. Leveraged **Linear Temporal Logic (LTL)** to verify protocol invariants and identified regression bugs in 20 minutes that had stalled cross-functional teams for weeks.
- **FIB Knowledge Recovery & Defensive Architecture:** Acted as the primary pioneer for the 6500-to-10.X control plane transition. Abstracted system identification methods to standardize topology launching across global teams. Resolved systemic memory corruption by refactoring undocumented legacy components and enforce **compile-time validation** guarding future code changes semantically.
- **Strategic AI Influence:** Featured speaker at Ciena's AI Forum. Contributed core tool-use orchestration and "Script-as-Tool" and **MCP** workflow to reduce LLM hallucinations. Created Agentic topology Validator using LLM-guided Genetic Programming.
- **2026 Unified DX Roadmap:** Spearheading a vision to unify Container, SIM, and HW lab environments through a **"Source-to-Source Topology Compiler,"** targeting a **50% reduction** in developer cognitive load by eliminating environment-specific configuration gaps.

Featured Project (Private Beta)

Clotho: Deterministic Interleaving Orchestrator for Concurrency Verification | ***Python, DPOR, AST Parsing***

- **Zero-modeling Verification:** Architected a verification engine that extracts concurrency topologies from uninstrumented code via **AST-level hijacking**, bypassing the need for manual formal modeling (e.g., TLA+/Promela).
- **Source-DPOR Implementation:** Implemented a scheduler to prune $O(N!)$ interleavings into $O(2^C)$ Mazurkiewicz equivalence classes; utilized **Vector Clocks** to maintain the lattice of global states without a synchronized clock.
- **RMW Semantic Decomposition:** Engineered a UniversalCausalTransformer using ast.NodeTransformer to desugar non-atomic Python primitives (e.g., $+=$) into explicit **Read-Modify-Write (RMW) yield points**, exposing hidden lost-update anomalies to the scheduler.
- **Transactional Time-Travel:** Achieved $O(1)$ **state restoration** by repurposing **SQLite SAVEPOINTs** as transactional memory; implemented rolling **XOR-based** state fingerprinting to detect livelocks via Shannon entropy stagnation.
- **Causal Grounding:** Leveraged Vector Clocks to maintain a relativistic partial order of events, ensuring deterministic replay of concurrent bugs by enforcing Lamport's happens-before relations across distributed component mocks.

Education

University of Waterloo Waterloo, ON
BASc in Computer Engineering (Honors, Graduated with Distinction) *Sept 2018 – Apr 2023*

- **GPA: 82.6/100**. Final Year Design Project StarCraft II AI Top 7 ranking in 2021 AI Arena.
- **Co-op Achievement**: Completed 5 merit-based internship terms (20 months) with a progressive focus on system complexity:
  - **Arctic Wolf**: Reduced collision between consecutive log processing via DynamoDB data segmentation.
  - **Coherent Logix**: Ported MATLAB core IEEE 802.11n components to multi-core DSP via Assembly/C performance tuning.
  - **Achievers**: Designed asynchronous optimistic UI GCS signed URL workflows and Python micro-services queried by GraphQL.
  - **Axonify**: Optimized monolithic API resource usage and automated test suites (Selenium) during the 2 Co-op terms.